Table 10. STM32F722xx and STM32F723xx pin and ball definition

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	1	1	A2	1	C9	A2	A3	1	1	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, FMC_A23, EVENTOUT	-
-	2	2	A1	2	A10	A1	A2	2	2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-
-	3	3	B1	3	D9	B1	B2	3	3	PE4	I/O	FT	-	TRACED1, SPI4_NSS, SAI1_FS_A, FMC_A20, EVENTOUT	-
-	4	4	B2	4	E8	B2	B3	4	4	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, EVENTOUT	-
-	5	5	B3	5	B10	B3	B4	5	5	PE6	I/O	FT	-	TRACED3, TIM1_BKIN2, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, SAI2_MCK_B, FMC_A22, EVENTOUT	-
1	6	6	C1	6	C10	C1	C2	6	6	VBAT	S	-	-	-	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	-	D2	7	-	D2	-	-	7	PI8	I/O	FT	(2) (3)	EVENTOUT	RTC_TAMP2/ RTC_TS, WKUP5
2	7	7	D1	8	D10	D1	A1	7	8	PC13	I/O	FT	(2) (3)	EVENTOUT	RTC_TAMP1/ RTC_TS/ RTC_OUT, WKUP4
3	8	8	E1	9	E9	E1	B1	8	9	PC14-OSC32_IN(PC14)	I/O	FT	(2) (3)	EVENTOUT	OSC32_IN
4	9	9	F1	10	E10	F1	C1	9	10	PC15-OSC32_OUT(PC15)	I/O	FT	(2) (3)	EVENTOUT	OSC32_OUT
-	-	-	D3	11	-	D3	-	-	11	PI9	I/O	FT	-	UART4_RX, CAN1_RX, FMC_D30, EVENTOUT	-
-	-	-	E3	12	-	E3	-	-	12	PI10	I/O	FT	-	FMC_D31, EVENTOUT	-
-	-	-	E4	13	-	E4	-	-	13	PI11	I/O	FT	(4)	OTG_HS_ULPI_DIR, EVENTOUT	WKUP6
-	-	-	F2	14	-	F2	-	-	14	VSS	S	-	-	-	-
-	-	-	F3	15	-	F3	-	-	15	VDD	S	-	-	-	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	10	E2	16	-	E2	C3	10	16	PF0	I/O	FTf	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	-	11	H3	17	-	H3	C4	11	17	PF1	I/O	FTf	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	-	12	H2	18	-	H2	D4	12	18	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	13	J2	19	-	J2	E2	13	19	PF3	I/O	FT	-	FMC_A3, EVENTOUT	ADC3_IN9
-	-	14	J3	20	-	J3	E3	14	20	PF4	I/O	FT	-	FMC_A4, EVENTOUT	ADC3_IN14
-	-	15	K3	21	-	K3	E4	15	21	PF5	I/O	FT	-	FMC_A5, EVENTOUT	ADC3_IN15
-	10	16	G2	22	F9	G2	D2	16	22	VSS	S	-	-	-	-
-	11	17	G3	23	F10	G3	D3	17	23	VDD	S	-	-	-	-
-	-	18	K2	24	-	K2	F3	18	24	PF6	I/O	FT	-	TIM10_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, QUADSPI_BK1_IO3, EVENTOUT	ADC3_IN4
-	-	19	K1	25	-	K1	F2	19	25	PF7	I/O	FT	-	TIM11_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_TX, QUADSPI_BK1_IO2, EVENTOUT	ADC3_IN5

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	20	L3	26	-	L3	G3	20	26	PF8	I/O	FT	-	SPI5_MISO, SAI1_SCK_B, UART7_RTS, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	ADC3_IN6
-	-	21	L2	27	-	L2	G2	21	27	PF9	I/O	FT	-	SPI5_MOSI, SAI1_FS_B, UART7_CTS, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	ADC3_IN7
-	-	22	L1	28	-	L1	G1	22	28	PF10	I/O	FT	-	EVENTOUT	ADC3_IN8
5	12	23	G1	29	G10	G1	D1	23	29	PH0-OSC_IN	I/O	FT	-	EVENTOUT	OSC_IN[5]
6	13	24	H1	30	H10	H1	E1	24	30	PH1-OSC_OUT	I/O	FT	-	EVENTOUT	OSC_OUT[5]
7	14	25	J1	31	G9	J1	F1	25	31	NRST	I/O	RST	-	-	-
8	15	26	M2	32	F8	M2	H1	26	32	PC0	I/O	FT	(4) (5)	SAI2_FS_B, OTG_HS_ULPI_STP, FMC_SDNWE, EVENTOUT	ADC1_IN10, ADC2_IN10, ADC3_IN10
9	16	27	M3	33	H9	M3	H2	27	33	PC1	I/O	FT	(5)	TRACED0, SPI2_MOSI/I2S2_SD, SAI1_SD_A, EVENTOUT	ADC1_IN11, ADC2_IN11, ADC3_IN11, RTC_TAMP3, WKUP3

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
10	17	28	M4	34	J10	M4	H3	28	34	PC2	I/O	FT	(4) (5)	SPI2_MISO, OTG_HS_ULPI_DIR, FMC_SDNE0, EVENTOUT	ADC1_IN12, ADC2_IN12, ADC3_IN12
11	18	29	M5	35	F7	M5	H4	29	35	PC3	I/O	FT	(4) (5)	SPI2_MOSI/I2S2_SD, OTG_HS_ULPI_NXT, FMC_SDCKE0, EVENTOUT	ADC1_IN13, ADC2_IN13, ADC3_IN13
-	-	30	-	36	J7	-	F10	30	36	VDD	S	-	-	-	-
12	19	31	M1	37	K10	M1	J1	31	37	VSSA	S	-	-	-	-
-	-	-	N1	-	-	N1	K1	-	-	VREF-	S	-	-	-	-
13	20	32	P1	38	J9	P1	L1	32	38	VREF+	S	-	-	-	-
-	21	33	R1	39	K9	R1	M1	33	39	VDDA	S	-	-	-	-
14	22	34	N3	40	G8	N3	J2	34	40	PA0-WKUP	I/O	FT	(5) (6)	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, SAI2_SD_B, EVENTOUT	ADC1_IN0, ADC2_IN0, ADC3_IN0, WKUP1

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
15	23	35	N2	41	J8	N2	K2	35	41	PA1	I/O	FT	(5)	TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCK_B, EVENTOUT	ADC1_IN1, ADC2_IN1, ADC3_IN1
16	24	36	P2	42	H8	P2	L2	36	42	PA2	I/O	FT	(5)	TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, SAI2_SCK_B, EVENTOUT	ADC1_IN2, ADC2_IN2, ADC3_IN2, WKUP2
-	-	-	F4	43	-	F4	-	-	43	PH2	I/O	FT		LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, FMC_SDCKE0, EVENTOUT	-
-	-	-	G4	44	-	G4	-	-	44	PH3	I/O	FT	-	QUADSPI_BK2_IO1, SAI2_MCK_B, FMC_SDNE0, EVENTOUT	-
-	-	-	H4	45	-	H4	-	-	45	PH4	I/O	FTf	(4)	I2C2_SCL, OTG_HS_ULPI_NXT, EVENTOUT	-
-	-	-	J4	46	-	J4	-	-	46	PH5	I/O	FTf	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-
17	25	37	R2	47	H7	R2	M2	37	47	PA3	I/O	FT	(4) (5)	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, OTG_HS_ULPI_D0, EVENTOUT	ADC1_IN3, ADC2_IN3, ADC3_IN3
18	26	38	-	-	K8	-	G4	38	-	VSS	S	-	-	-	-
-	-	-	L4	48	-	L4	H5	-	48	BYPASS_REG	I	FT	-	-	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
19	27	39	K4	49	-	K4	F4	39	49	VDD	S	-	-	-	-
20	28	40	N4	50	G7	N4	J3	40	50	PA4	I/O	TTa	(5)	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, OTG_HS_SOF, EVENTOUT	ADC1_IN4, ADC2_IN4, DAC_OUT1
21	29	41	P4	51	F6	P4	K3	41	51	PA5	I/O	TTa	(4) (5)	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, OTG_HS_ULPI_CK, EVENTOUT	ADC1_IN5, ADC2_IN5, DAC_OUT2
22	30	42	P3	52	G6	P3	L3	42	52	PA6	I/O	FT	(5)	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM13_CH1, EVENTOUT	ADC1_IN6, ADC2_IN6
23	31	43	R3	53	K7	R3	M3	43	53	PA7	I/O	FT	(5)	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, TIM14_CH1, FMC_SDNWE, EVENTOUT	ADC1_IN7, ADC2_IN7
24	32	44	N5	54	H6	N5	J4	44	54	PC4	I/O	FT	(5)	I2S1_MCK, FMC_SDNE0, EVENTOUT	ADC1_IN14, ADC2_IN14
-	33	45	P5	55	J6	P5	K4	45	55	PC5	I/O	FT	(5)	FMC_SDCKE0, EVENTOUT	ADC1_IN15, ADC2_IN15

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
25	34	46	R5	56	F5	R5	L4	46	56	PB0	I/O	FT	(4) (5)	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, UART4_CTS, OTG_HS_ULPI_D1, EVENTOUT	ADC1_IN8, ADC2_IN8
26	35	47	R4	57	G5	R4	M4	47	57	PB1	I/O	FT	(4) (5)	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, OTG_HS_ULPI_D2, EVENTOUT	ADC1_IN9, ADC2_IN9
27	36	48	M6	58	K6	M6	J5	48	58	PB2	I/O	FT	-	SAI1_SD_A, SPI3_MOSI/I2S3_SD, QUADSPI_CLK, EVENTOUT	-
-	-	49	R6	59	-	R6	M5	49	59	PF11	I/O	FT	-	SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, EVENTOUT	-
-	-	50	P6	60	-	P6	L5	50	60	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	-	51	M8	61	-	M8	-	51	61	VSS	S	-	-	-	-
-	-	52	N8	62	-	N8	G5	52	62	VDD	S	-	-	-	-
-	-	53	N6	63	-	N6	K5	53	63	PF13	I/O	FT	-	FMC_A7, EVENTOUT	-
-	-	54	R7	64	-	R7	M6	54	64	PF14	I/O	FT	-	FMC_A8, EVENTOUT	-
-	-	55	P7	65	-	P7	L6	55	65	PF15	I/O	FT	-	FMC_A9, EVENTOUT	-
-	-	56	N7	66	-	N7	K6	56	66	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	-	57	M7	67	-	M7	J6	57	67	PG1	I/O	FT	-	FMC_A11, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	37	58	R8	68	J5	R8	M7	58	68	PE7	I/O	FT	-	TIM1_ETR, UART7_Rx, QUADSPI_BK2_IO0, FMC_D4, EVENTOUT	-
-	38	59	P8	69	H5	P8	L7	59	69	PE8	I/O	FT	-	TIM1_CH1N, UART7_Tx, QUADSPI_BK2_IO1, FMC_D5, EVENTOUT	-
-	39	60	P9	70	K5	P9	K7	60	70	PE9	I/O	FT	-	TIM1_CH1, UART7_RTS, QUADSPI_BK2_IO2, FMC_D6, EVENTOUT	-
-	-	61	M9	71	-	M9	H6	61	71	VSS	S	-	-	-	-
-	-	62	N9	72	-	N9	G6	62	72	VDD	S	-	-	-	-
-	40	63	R9	73	E4	R9	J7	63	73	PE10	I/O	FT	-	TIM1_CH2N, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7, EVENTOUT	-
-	41	64	P10	74	G4	P10	H8	64	74	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS, SAI2_SD_B, FMC_D8, EVENTOUT	-
-	42	65	R10	75	H4	R10	J8	65	75	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK, SAI2_SCK_B, FMC_D9, EVENTOUT	-
-	43	66	N11	76	J4	N11	K8	66	76	PE13	I/O	FT	-	TIM1_CH3, SPI4_MISO, SAI2_FS_B, FMC_D10, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	44	67	P11	77	K4	P11	L8	67	77	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI, SAI2_MCK_B, FMC_D11,, EVENTOUT	-
-	45	68	R11	78	F4	R11	M8	68	78	PE15	I/O	FT	-	TIM1_BKIN, FMC_D12, EVENTOUT	-
28	46	69	R12	79	G3	R12	M9	69	79	PB10	I/O	FTf	(4)	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, USART3_TX, OTG_HS_ULPI_D3, EVENTOUT	-
29	47	70	R13	80	H3	R13	M10	70	80	PB11	I/O	FTf	(4)	TIM2_CH4, I2C2_SDA, USART3_RX, OTG_HS_ULPI_D4, EVENTOUT	-
30	48	71	M10	81	J3	M10	H7	71	81	VCAP_1	S	-	-	-	-
31	49	-	-	-	K3	-	-	-	-	VSS	S	-	-	-	-
32	50	72	N10	82	K2	N10	G7	72	82	VDD	S	-	-	-	-
-	-	-	M11	83	-	M11	-	-	83	PH6	I/O	FT	-	I2C2_SMBA, SPI5_SCK, TIM12_CH1, FMC_SDNE1, EVENTOUT	-
-	-	-	N12	84	-	N12	-	-	84	PH7	I/O	FTf	-	I2C3_SCL, SPI5_MISO, FMC_SDCKE1, EVENTOUT	-
-	-	-	M12	85	-	M12	-	-	85	PH8	I/O	FTf	-	I2C3_SDA, FMC_D16, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	-	M13	86	-	M13	-	-	86	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, FMC_D17, EVENTOUT	-
-	-	-	L13	87	-	L13	-	-	87	PH10	I/O	FT	-	TIM5_CH1, FMC_D18, EVENTOUT	-
-	-	-	L12	88	-	L12	-	-	88	PH11	I/O	FT	-	TIM5_CH2, FMC_D19, EVENTOUT	-
-	-	-	K12	89	-	K12	-	-	89	PH12	I/O	FT	-	TIM5_CH3, FMC_D20, EVENTOUT	-
-	-	-	H12	90	-	H12	-	-	90	VSS	S	-	-	-	-
-	-	-	J12	91	K2	J12	-	-	91	VDD	S	-	-	-	-
33	51	73	P12	92	J2	P12	M11	73	92	PB12	I/O	FT	(4)	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, OTG_HS_ULPI_D5, OTG_HS_ID, EVENTOUT	-
34	52	74	P13	93	H2	P13	M12	74	93	PB13	I/O	FT	(4)	TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, OTG_HS_ULPI_D6, EVENTOUT	OTG_HS_VBUS
-	-	-	-	-	G2	J15	H11	75	94	OTG_HS_REXT	-	-	-	USB HS OTG PHY calibration resistor	
-	-	-	-	-	G1	J14	H10	76	95	VDD12OTGHS	-	-	-	-	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
35	53	75	R14	94	-	-	-	-	-	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, SPI2_MISO, USART3_RTS, TIM12_CH1, SDMMC2_D0, OTG_HS_DM, EVENTOUT	-
-	-	-	-	-	J1	R14	L11	77	96	PB14	I/O	FT	-	OTG_HS_DM	-
36	54	76	R15	95	-	-	-	-	-	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI/I2S2_SD, TIM12_CH2, SDMMC2_D1, OTG_HS_DP, EVENTOUT	-
-	-	-	-	-	H1	R15	L12	78	97	PB15	I/O	FT	-	OTG_HS_DP	-
-	55	77	P15	96	-	P15	L9	79	98	PD8	I/O	FT	-	USART3_TX, FMC_D13, EVENTOUT	-
-	56	78	P14	97	-	P14	K9	80	99	PD9	I/O	FT	-	USART3_RX, FMC_D14, EVENTOUT	-
-	57	79	N15	98	-	N15	J9	81	100	PD10	I/O	FT	-	USART3_CK, FMC_D15, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	58	80	N14	99	F3	N14	H9	82	101	PD11	I/O	FT	-	USART3_CTS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16/FMC_CLE, EVENTOUT	-
-	59	81	N13	100	F2	N13	L10	83	102	PD12	I/O	FT	-	TIM4_CH1, LPTIM1_IN1, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17/FMC_ALE, EVENTOUT	-
-	60	82	M15	101	E3	M15	K10	84	103	PD13	I/O	FT	-	TIM4_CH2, LPTIM1_OUT, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-
-	-	83	-	102	-	-	G8	85	104	VSS	S	-	-	-	-
-	-	84	J13	103	-	J13	F8	86	105	VDD	S	-	-	-	-
-	61	85	M14	104	F1	M14	K11	87	106	PD14	I/O	FT	-	TIM4_CH3, UART8_CTS, FMC_D0, EVENTOUT	-
-	62	86	L14	105	E2	L14	K12	88	107	PD15	I/O	FT	-	TIM4_CH4, UART8_RTS, FMC_D1, EVENTOUT	-
-	-	87	L15	106	-	L15	J12	89	108	PG2	I/O	FT	-	FMC_A12, EVENTOUT	-
-	-	88	K15	107	-	K15	J11	90	109	PG3	I/O	FT	-	FMC_A13, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	89	K14	108	-	K14	J10	91	110	PG4	I/O	FT	-	FMC_A14/FMC_BA0, EVENTOUT	-
-	-	90	K13	109	-	K13	H12	92	111	PG5	I/O	FT	-	FMC_A15/FMC_BA1, EVENTOUT	-
-	-	91	J15	110	-	-	-	-	-	PG6	I/O	FT	-	EVENTOUT	-
-	-	92	J14	111	-	-	-	-	-	PG7	I/O	FT	-	USART6_CK, FMC_INT, EVENTOUT	-
-	-	93	H14	112	-	H14	G11	93	112	PG8	I/O	FT	-	USART6_RTS, FMC_SDCLK, EVENTOUT	-
-	-	94	G12	113	-	G12	-	94	113	VSS	S	-	-	-	-
					-	-	F10	-	-	VDD					
-	-	95	H13	114	K1	H13	C11	95	114	VDDUSB	S	-	-	-	-
37	63	96	H15	115	E1	H15	G12	96	115	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, USART6_TX, SDMMC2_D6, SDMMC1_D6, EVENTOUT	-
38	64	97	G15	116	D4	G15	F12	97	116	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, SDMMC2_D7, SDMMC1_D7, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
39	65	98	G14	117	D2	G14	F11	98	117	PC8	I/O	FT	-	TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, SDMMC1_D0, EVENTOUT	-
40	66	99	F14	118	D1	F14	E11	99	118	PC9	I/O	FTf	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, SDMMC1_D1, EVENTOUT	-
41	67	100	F15	119	D3	F15	E12	100	119	PA8	I/O	FTf	-	MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, EVENTOUT	-
42	68	101	E15	120	C3	E15	D12	101	120	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, EVENTOUT	OTG_FS_VBUS
43	69	102	D15	121	C2	D15	D11	102	121	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, EVENTOUT	-
44	70	103	C15	122	C1	C15	C12	103	122	PA11	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, EVENTOUT	-
45	71	104	B15	123	B2	B15	B12	104	123	PA12	I/O	FT	-	TIM1_ETR, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, EVENTOUT	-
46	72	105	A15	124	B1	A15	A12	105	124	PA13(JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	73	106	F13	125	B3	F13	G9	106	125	VCAP_2	S	-	-	-	-
47	74	107	F12	126	A2	F12	G10	107	126	VSS	S	-	-	-	-
48	75	108	G13	127	A1	G13	F9	108	127	VDD	S	-	-	-	-
-	-	-	E12	128	-	E12	-	-	128	PH13	I/O	FT	-	TIM8_CH1N, UART4_TX, CAN1_TX, FMC_D21, EVENTOUT	-
-	-	-	E13	129	-	E13	-	-	129	PH14	I/O	FT	-	TIM8_CH2N, UART4_RX, CAN1_RX, FMC_D22, EVENTOUT	-
-	-	-	D13	130	-	D13	-	-	130	PH15	I/O	FT	-	TIM8_CH3N, FMC_D23, EVENTOUT	-
-	-	-	E14	131	-	E14	-	-	131	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS, FMC_D24, EVENTOUT	-
-	-	-	D14	132	-	D14	-	-	132	PI1	I/O	FT	-	TIM8_BKIN2, SPI2_SCK/I2S2_CK, FMC_D25, EVENTOUT	-
-	-	-	C14	133	-	C14	-	-	133	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, FMC_D26, EVENTOUT	-
-	-	-	C13	134	-	C13	-	-	134	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, EVENTOUT	-
-	-	-	D9	135	-	D9	-	-	135	VSS	S	-	-	-	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	-	C9	136	-	C9	-	-	136	VDD	S	-	-	-	-
49	76	109	A14	137	C4	A14	A11	109	137	PA14(JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
50	77	110	A13	138	B4	A13	A10	110	138	PA15(JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, UART4_RTS, EVENTOUT	-
51	78	111	B14	139	A3	B14	B11	111	139	PC10	I/O	FT	-	SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, EVENTOUT	-
52	79	112	B13	140	C5	B13	B10	112	140	PC11	I/O	FT	-	SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC1_D3, EVENTOUT	-
53	80	113	A12	141	D5	A12	C10	113	141	PC12	I/O	FT	-	TRACED3, SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDMMC1_CK, EVENTOUT	-
-	81	114	B12	142	B5	B12	E10	114	142	PD0	I/O	FT	-	CAN1_RX, FMC_D2, EVENTOUT	-
-	82	115	C12	143	A4	C12	D10	115	143	PD1	I/O	FT	-	CAN1_TX, FMC_D3, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
54	83	116	D12	144	E5	D12	E9	116	144	PD2	I/O	FT	-	TRACED2, TIM3_ETR, UART5_RX, SDMMC1_CMD, EVENTOUT	-
-	84	117	D11	145	C6	D11	D9	117	145	PD3	I/O	FT	-	SPI2_SCK/I2S2_CK, USART2_CTS, FMC_CLK, EVENTOUT	-
-	85	118	D10	146	B6	D10	C9	118	146	PD4	I/O	FT	-	USART2_RTS, FMC_NOE, EVENTOUT	-
-	86	119	C11	147	A5	C11	B9	119	147	PD5	I/O	FT	-	USART2_TX, FMC_NWE, EVENTOUT	-
-	-	120	D8	148	-	D8	E7	120	148	VSS	S	-	-	-	-
-	-	121	C8	149	-	C8	F7	121	149	VDDSDMMC	S	-	-	-	-
-	87	122	B11	150	D6	B11	A8	122	150	PD6	I/O	FT	-	SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, SDMMC2_CK, FMC_NWAIT, EVENTOUT	-
-	88	123	A11	151	E6	A11	A9	123	151	PD7	I/O	FT	-	USART2_CK SDMMC2_CMD, FMC_NE1, EVENTOUT	-
-	-	124	C10	152	-	C10	E8	124	152	PG9	I/O	FT	-	USART6_RX, QUADSPI_BK2_IO2, SAI2_FS_B, SDMMC2_D0, FMC_NE2/FMC_NCE, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	125	B10	153	-	B10	D8	125	153	PG10	I/O	FT	-	SAI2_SD_B, SDMMC2_D1, FMC_NE3, EVENTOUT	-
-	-	126	B9	154	-	B9	C8	126	154	PG11	I/O	FT	-	SDMMC2_D2, FMC_INT, EVENTOUT	-
-	-	127	B8	155	-	B8	B8	127	155	PG12	I/O	FT	-	LPTIM1_IN1, USART6_RTS, SDMMC2_D3, FMC_NE4, EVENTOUT	-
-	-	128	A8	156	-	A8	D7	128	156	PG13	I/O	FT	-	TRACED0, LPTIM1_OUT, USART6_CTS, FMC_A24, EVENTOUT	-
-	-	129	A7	157	-	A7	C7	129	157	PG14	I/O	FT	-	TRACED1, LPTIM1_ETR, USART6_TX, QUADSPI_BK2_IO3, FMC_A25, EVENTOUT	-
-	-	130	D7	158	-	D7	-	130	158	VSS	S	-	-	-	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	131	C7	159	-	C7	F6	131	159	VDD	S	-	-	-	-
-	-	132	B7	160	-	B7	B7	132	160	PG15	I/O	FT	-	USART6_CTS, FMC_SDNCAS, EVENTOUT	-
55	89	133	A10	161	A6	A10	A7	133	161	PB3(JTDO/TRACESWO)	I/O	FT	-	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, SDMMC2_D2, EVENTOUT	-
56	90	134	A9	162	B7	A9	A6	134	162	PB4(NJTRST)	I/O	FT	-	NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, SPI2_NSS/I2S2_WS, SDMMC2_D3, EVENTOUT	-
57	91	135	A6	163	C7	A6	B6	135	163	PB5	I/O	FT	(4)	TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, OTG_HS_ULPI_D7, FMC_SDCKE1, EVENTOUT	-
58	92	136	B6	164	D7	B6	C6	136	164	PB6	I/O	FTf	-	TIM4_CH1, I2C1_SCL, USART1_TX, QUAD SPI_BK1_NCS, FMC_SDNE1, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
59	93	137	B5	165	B8	B5	D6	137	165	PB7	I/O	FTf	-	TIM4_CH2, I2C1_SDA, USART1_RX, FMC_NL, EVENTOUT	-
60	94	138	D6	166	A7	D6	D5	138	166	BOOT	I	B	-	-	VPP
61	95	139	A5	167	C8	A5	C5	139	167	PB8	I/O	FTf	-	TIM4_CH3, TIM10_CH1, I2C1_SCL, CAN1_RX, SDMMC2_D4, SDMMC1_D4, EVENTOUT	-
62	96	140	B4	168	D8	B4	B5	140	168	PB9	I/O	FTf	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, SDMMC2_D5, SDMMC1_D5, EVENTOUT	-
-	97	141	A4	169	E7	A4	A5	141	169	PE0	I/O	FT	-	TIM4_ETR, LPTIM1_ETR, UART8_Rx, SAI2_MCK_A, FMC_NBL0, EVENTOUT	-
-	98	142	A3	170	B9	A3	A4	142	170	PE1	I/O	FT	-	LPTIM1_IN2, UART8_Tx, FMC_NBL1, EVENTOUT	-
63	99	-	D5	-	A8	D5	E6	-	-	VSS	S	-	-	-	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	143	C6	171	-	C6	E5	143	171	PDR_ON	S	-	-	-	-
64	100	144	C5	172	A9	C5	F5	144	172	VDD	S	-	-	-	-
-	-	-	D4	173	-	D4	-	-	173	PI4	I/O	FT	-	TIM8_BKIN, SAI2_MCK_A, FMC_NBL2, EVENTOUT	-
-	-	-	C4	174	-	C4	-	-	174	PI5	I/O	FT	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, EVENTOUT	-
-	-	-	C3	175	-	C3	-	-	175	PI6	I/O	FT	-	TIM8_CH2, SAI2_SD_A, FMC_D28, EVENTOUT	-
-	-	-	C2	176	-	C2	-	-	176	PI7	I/O	FT	-	TIM8_CH3, SAI2_FS_A, FMC_D29, EVENTOUT	-
-	-	-	F6	-	-	F6	-	-	-	VSS	S	-	-	-	-
-	-	-	F7	-	-	F7	-	-	-	VSS	S	-	-	-	-
-	-	-	F8	-	-	F8	-	-	-	VSS	S	-	-	-	-
-	-	-	F9	-	-	F9	-	-	-	VSS	S	-	-	-	-
-	-	-	F10	-	-	F10	-	-	-	VSS	S	-	-	-	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	-	G6	-	-	G6	-	-	-	VSS	S	-	-	-	-
-	-	-	G7	-	-	G7	-	-	-	VSS	S	-	-	-	-
-	-	-	G8	-	-	G8	-	-	-	VSS	S	-	-	-	-
-	-	-	G9	-	-	G9	-	-	-	VSS	S	-	-	-	-
-	-	-	G10	-	-	G10	-	-	-	VSS	S	-	-	-	-
-	-	-	H6	-	-	H6	-	-	-	VSS	S	-	-	-	-
-	-	-	H7	-	-	H7	-	-	-	VSS	S	-	-	-	-
-	-	-	H8	-	-	H8	-	-	-	VSS	S	-	-	-	-
-	-	-	H9	-	-	H9	-	-	-	VSS	S	-	-	-	-
-	-	-	H10	-	-	H10	-	-	-	VSS	S	-	-	-	-
-	-	-	J6	-	-	J6	-	-	-	VSS	S	-	-	-	-
-	-	-	J7	-	-	J7	-	-	-	VSS	S	-	-	-	-
-	-	-	J8	-	-	J8	-	-	-	VSS	S	-	-	-	-
-	-	-	J9	-	-	J9	-	-	-	VSS	S	-	-	-	-
-	-	-	J10	-	-	J10	-	-	-	VSS	S	-	-	-	-
-	-	-	K6	-	-	K6	-	-	-	VSS	S	-	-	-	-
-	-	-	K7	-	-	K7	-	-	-	VSS	S	-	-	-	-
-	-	-	K8	-	-	K8	-	-	-	VSS	S	-	-	-	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	-	K9	-	-	K9	-	-	-	VSS	S	-	-	-	-
-	-	-	K10	-	-	K10	-	-	-	VSS	S	-	-	-	-

1. Function availability depends on the chosen device.
2. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset).
4. ULPI signals not available on the STM32F723xx devices.
5. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
6. If the device is in regulator OFF/internal reset ON mode (BYPASS_REG pin is set to VDD), then PA0 is used as an internal reset (active low).

The 8 requests from the peripherals (TIM, ADC, SPI, I2C, etc.) are independently connected to each channel and their connection depends on the product implementation.

Table 25 and *Table 26* give examples of DMA request mappings.

Table 25. DMA1 request mapping

Peripheral requests	Stream 0	Stream 1	Stream 2	Stream 3	Stream 4	Stream 5	Stream 6	Stream 7
Channel 0	SPI3_RX	-	SPI3_RX	SPI2_RX	SPI2_TX	SPI3_TX	-	SPI3_TX
Channel 1	I2C1_RX	I2C3_RX	TIM7_UP		TIM7_UP	I2C1_RX	I2C1_TX	I2C1_TX
Channel 2	TIM4_CH1	-	-	TIM4_CH2	-	-	TIM4_UP	TIM4_CH3
Channel 3	-	TIM2_UP TIM2_CH3	I2C3_RX	-	I2C3_TX	TIM2_CH1	TIM2_CH2 TIM2_CH4	TIM2_UP TIM2_CH4
Channel 4	UART5_RX	USART3_RX	UART4_RX	USART3_TX	UART4_TX	USART2_RX	USART2_TX	UART5_TX
Channel 5	UART8_TX	UART7_TX	TIM3_CH4 TIM3_UP	UART7_RX	TIM3_CH1 TIM3_TRIG	TIM3_CH2	UART8_RX	TIM3_CH3
Channel 6	TIM5_CH3 TIM5_UP	TIM5_CH4 TIM5_TRIG	TIM5_CH1	TIM5_CH4 TIM5_TRIG	TIM5_CH2	-	TIM5_UP	-
Channel 7	-	TIM6_UP	I2C2_RX	I2C2_RX	USART3_TX	DAC1	DAC2	I2C2_TX

Table 26. DMA2 request mapping

Peripheral requests	Stream 0	Stream 1	Stream 2	Stream 3	Stream 4	Stream 5	Stream 6	Stream 7
Channel 0	ADC1	SAI1_A	TIM8_CH1 TIM8_CH2 TIM8_CH3	SAI1_A	ADC1	SAI1_B	TIM1_CH1 TIM1_CH2 TIM1_CH3	SAI2_B
Channel 1	-	-	ADC2	ADC2	SAI1_B	-	-	-
Channel 2	ADC3	ADC3	-	SPI5_RX	SPI5_TX	AES_OUT	AES_IN	-
Channel 3	SPI1_RX	-	SPI1_RX	SPI1_TX	SAI2_A	SPI1_TX	SAI2_B	QUADSPI
Channel 4	SPI4_RX	SPI4_TX	USART1_RX	SDMMC1	-	USART1_RX	SDMMC1	USART1_TX
Channel 5	-	USART6_RX	USART6_RX	SPI4_RX	SPI4_TX	-	USART6_TX	USART6_TX
Channel 6	TIM1_TRIG	TIM1_CH1	TIM1_CH2	TIM1_CH1	TIM1_CH4 TIM1_TRIG TIM1_COM	TIM1_UP	TIM1_CH3	-
Channel 7	-	TIM8_UP	TIM8_CH1	TIM8_CH2	TIM8_CH3	SPI5_RX	SPI5_TX	TIM8_CH4 TIM8_TRIG TIM8_COM
Channel 11	SDMMC2	-	-	-	-	SDMMC2	-	-