Table 9. Pin/ball definition

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
1	A3	1	A2	A2	1	1	C3	PE2	I/O	FT_h	-	TRACECLK, SAI1_CK1, SPI4_SCK, SAI1_MCLK_A, SAI4_MCLK_A, QUADSPI_BK1_IO2, SAI4_CK1, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
2	B3	2	B2	A1	2	2	D3	PE3	I/O	FT_h	-	TRACED0, TIM15_BKIN, SAI1_SD_B, SAI4_SD_B, FMC_A19, EVENTOUT	-
3	C3	3	A1	B1	3	3	D2	PE4	I/O	FT_h	-	TRACED1, SAI1_D2, DFSDM1_DATIN3, TIM15_CH1N, SPI4_NSS, SAI1_FS_A, SAI4_FS_A, SAI4_D2, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT	-
4	D3	4	C3	B2	4	4	D1	PE5	I/O	FT_h	-	TRACED2, SAI1_CK2, DFSDM1_CKIN3, TIM15_CH1, SPI4_MISO, SAI1_SCK_A, SAI4_SCK_A, SAI4_CK2, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT	-
5	E3	5	C2	B3	5	5	E5	PE6	I/O	FT_h	-	TRACED3, TIM1_BKIN2, SAI1_D1, TIM15_CH2, SPI4_MOSI, SAI1_SD_A, SAI4_SD_A, SAI4_D1, SAI2_MCLK_B, TIM1_BKIN2_COMP12, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT	-
-	-	-	M4	H10	-	-	A1	VSS	S	-	-	-	-
-	-	-	A3	-	-	-	-	VDD	S	-	-	-	-
6	B2	6	E3	C1	6	6	B1	VBAT	S	-	-	-	-
-	-	-	-	J6	-	-	B2	VSS	S	-	-	-	-
-	-	-	-	D2	7	7	E4	PI8	I/O	FT	-	EVENTOUT	RTC_TAMP2/ WKUP3
7	A2	7	D3	D1	8	8	E3	PC13	I/O	FT	-	EVENTOUT	RTC_TAMP1/ RTC_TS/ WKUP2
-	-	-	-	J7	-	-	B6	VSS	S	-	-	-	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
8	A1	8	C1	E1	9	9	C2	PC14-OSC32_IN (OSC32_IN)(1)	I/O	FT	-	EVENTOUT	OSC32_IN
9	B1	9	B1	F1	10	10	C1	PC15-OSC32_OUT (OSC32_OUT)(1)	I/O	FT	-	EVENTOUT	OSC32_OUT
-	-	-	-	D3	11	11	E2	PI9	I/O	FT_h	-	UART4_RX, FDCAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-
-	-	-	-	E3	12	12	F3	PI10	I/O	FT_h	-	FDCAN1_RXFD_MODE, ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT	
-	-	-	E1	E4	13	13	F4	PI11	I/O	FT	-	LCD_G6, OTG_HS_ULPI_DIR, EVENTOUT	WKUP4
-	C2	-	D2	F2	14	14	A17	VSS	S	-	-	-	-
-	D2	-	D1	F3	15	15	E6	VDD	S	-	-	-	-
-	-	-	-	-	-	-	E1(2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	F1(3)	NC	-	-	-	-	-
-	-	-	-	-	-	-	G2(4)	NC	-	-	-	-	-
-	-	10	F3	E2	16	16	G4	PF0	I/O	FT_f	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	-	11	E4	H3	17	17	G3	PF1	I/O	FT_f	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	-	12	F4	H2	18	18	G1	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	F2	-	-	19	H1	PI12	I/O	FT	-	LCD_HSYNC, EVENTOUT	-
-	-	-	F1	-	-	20	H2	PI13	I/O	FT	-	LCD_VSYNC, EVENTOUT	-
-	-	-	-	-	-	21	H3	PI14	I/O	FT_h	-	LCD_CLK, EVENTOUT	-
-	-	13	E5	J2	19	22	H4	PF3	I/O	FT_ha	-	FMC_A3, EVENTOUT	ADC3_INP5

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	14	G3	J3	20	23	J5	PF4	I/O	FT_ha	-	FMC_A4, EVENTOUT	ADC3_INN5, ADC3_INP9
-	-	15	F5	K3	21	24	J4	PF5	I/O	FT_ha	-	FMC_A5, EVENTOUT	ADC3_INP4
10	-	16	B10	G2	22	25	C10	VSS	S	-	-	-	-
11	-	17	G1	G3	23	26	E9	VDD	S	-	-	-	-
-	-	18	G4	K2	24	27	K2	PF6	I/O	FT_ha	-	TIM16_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, SAI4_SD_B, QUADSPI_BK1_IO3, EVENTOUT	ADC3_INN4, ADC3_INP8
-	-	19	F6	K1	25	28	K3	PF7	I/O	FT_ha	-	TIM17_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_TX, SAI4_MCLK_B, QUADSPI_BK1_IO2, EVENTOUT	ADC3_INP3
-	-	20	H4	L3	26	29	K4	PF8	I/O	FT_ha	-	TIM16_CH1N, SPI5_MISO, SAI1_SCK_B, UART7_RTS/UART7_DE, SAI4_SCK_B, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	ADC3_INN3, ADC3_INP7
-	-	21	G5	L2	27	30	L4	PF9	I/O	FT_ha	-	TIM17_CH1N, SPI5_MOSI, SAI1_FS_B, UART7_CTS, SAI4_FS_B, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	ADC3_INP2
-	-	22	H3	L1	28	31	L3	PF10	I/O	FT_ha	-	TIM16_BKIN, SAI1_D3, QUADSPI_CLK, SAI4_D3, DCMI_D11, LCD_DE, EVENTOUT	ADC3_INN2, ADC3_INP6
12	C1	23	H1	G1	29	32	J2	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
13	D1	24	H2	H1	30	33	J1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
14	E1	25	G6	J1	31	34	K1	NRST	I/O	RST	-	-	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
15	F1	26	J1	M2	32	35	L2	PC0	I/O	FT_a	-	DFSDM1_CKIN0, DFSDM1_DATIN4, SAI2_FS_B, OTG_HS_ULPI_STP, FMC_SDNWE, LCD_R5, EVENTOUT	ADC123_ INP10
16	F2	27	J2	M3	33	36	M2	PC1	I/O	FT_ ha	-	TRACED0, SAI1_D1, DFSDM1_DATIN0, DFSDM1_CKIN4, SPI2_MOSI/I2S2_SDO, SAI1_SD_A, SAI4_SD_A, SDMMC2_CK, SAI4_D1, ETH_MDC, MDIOS_MDC, EVENTOUT	ADC123_ INN10, ADC123_ INP11, RTC_TAMP3/W KUP5
-	-	-	-	-	-	-	M3(5)	PC2	I/O	FT_a	-	CDSLEEP, DFSDM1_CKIN1, SPI2_MISO/I2S2_SDI, DFSDM1_CKOUT, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC123_ INN11, ADC123_ INP12
17 (6)	E2(6)	28(6)	K2(6)	M4(6)	34(6)	37(6)	R1(5)	PC2_C	ANA	TT_a	-		ADC3_INN1, ADC3_INP0
-	-	-	-	-	-	-	M4(5)	PC3	I/O	FT_a	-	CSLEEP, DFSDM1_DATIN1, SPI2_MOSI/I2S2_SDO, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC12_INN12, ADC12_INP13
18 (6)	F3(6)	29(6)	K1(6)	M5(6)	35(6)	38(6)	R2(5)	PC3_C	ANA	TT_a	-		ADC3_INP1
-	F5	30	-	G3	36	39	E11	VDD	S	-	-	-	-
-	E6	-	B3	J10	-	-	C13	VSS	S	-	-	-	-
19	G1	31	J3	M1	37	40	P1	VSSA	S	-	-	-	-
-	-	-	-	N1	-	-	N1	VREF-	S	-	-	-	-
20	-(7)	32	L2	P1	38	41	M1	VREF+	S	-	-	-	-
21	H1	33	L1	R1	39	42	L1	VDDA	S	-	-	-	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
22	G2	34	J5	N3	40	43	N5(5)	PA0	I/O	FT_a	-	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, TIM15_BKIN, USART2_CTS/USART2_NSS, UART4_TX, SDMMC2_CMD, SAI2_SD_B, ETH_MII_CRS, EVENTOUT	ADC1_INP16, WKUP0
-	-	-	-	-	-	-	T1(5)	PA0_C	ANA	TT_a	-		ADC12_INN1, ADC12_INP0
23	H2	35	K4	N2	41	44	N4(5)	PA1	I/O	FT_ha	-	TIM2_CH2, TIM5_CH2, LPTIM3_OUT, TIM15_CH1N, USART2_RTS/USART2_DE, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCLK_B, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, LCD_R2, EVENTOUT	ADC1_INN16, ADC1_INP17
-	-	-	-	-	-	-	T2(5)	PA1_C	ANA	TT_a	-		ADC12_INP1
24	J2	36	N1	P2	42	45	N3	PA2	I/O	FT_a	-	TIM2_CH3, TIM5_CH3, LPTIM4_OUT, TIM15_CH1, USART2_TX, SAI2_SCK_B, ETH_MDIO, MDIOS_MDIO, LCD_R1, EVENTOUT	ADC12_INP14, WKUP1
-	-	-	N2	F4	43	46	N2	PH2	I/O	FT_ha	-	LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT	ADC3_INP13
-	K1	-	M1	-	-	-	F5	VDD	S	-	-	-	-
-	J1	-	M7	J8	-	-	C16	VSS	S	-	-	-	-
-	-	-	M3	G4	44	47	P2	PH3	I/O	FT_ha	-	QUADSPI_BK2_IO1, SAI2_MCLK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	ADC3_INN13, ADC3_INP14
-	-	-	K3	H4	45	48	P3	PH4	I/O	FT_fa	-	I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, LCD_G4, EVENTOUT	ADC3_INN14, ADC3_INP15
-	-	-	L3	J4	46	49	P4	PH5	I/O	FT_fa	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	ADC3_INN15, ADC3_INP16

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
25	K2	37	N3	R2	47	50	U2	PA3	I/O	FT_ha	-	TIM2_CH4, TIM5_CH4, LPTIM5_OUT, TIM15_CH2, USART2_RX, LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC12_INP15
26	-	38	G2	K6	-	51	F2(4)	VSS	S	-	-	-	-
-	-	-	-	L4	48	-	-	VSS	S	-	-	-	-
27	-	39	-	K4	49	52	G5	VDD	S	-	-	-	-
28	G3	40	H6	N4	50	53	U3	PA4	I/O	TT_a	-	D1PWREN, TIM5_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_INP18, DAC1_OUT1
29	H3	41	L4	P4	51	54	T3	PA5	I/O	TT_ha	-	D2PWREN, TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC12_INN18, ADC12_INP19, DAC1_OUT2
30	J3	42	K5	P3	52	55	R3	PA6	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO/I2S1_SDI, SPI6_MISO, TIM13_CH1, TIM8_BKIN_COMP12, MDIOS_MDC, TIM1_BKIN_COMP12, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_INP3
31	K3	43	J6	R3	53	56	R5	PA7	I/O	TT_a	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SDO, SPI6_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC12_INN3, ADC12_INP7, OPAMP1_VINM

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
32	G4	44	K6	N5	54	57	T4	PC4	I/O	TT_a	-	DFSDM1_CKIN2, I2S1_MCK, SPDIFRX1_IN3, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT	ADC12_INP4, OPAMP1_VOUT, COMP1_INM
33	H4	45	N5	P5	55	58	U4	PC5	I/O	TT_a	-	SAI1_D3, DFSDM1_DATIN2, SPDIFRX1_IN4, SAI4_D3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, COMP1_OUT, EVENTOUT	ADC12_INN4, ADC12_INP8, OPAMP1_VINM
-	-	-	N4	-	-	59	G13	VDD	S	-	-	-	-
-	-	-	H12	J9	-	60	R4	VSS	S	-	-	-	-
34	J4	46	M5	R5	56	61	U5	PB0	I/O	FT_a	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, DFSDM1_CKOUT, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT	ADC12_INN5, ADC12_INP9, OPAMP1_VINP, COMP1_INP
35	K4	47	L5	R4	57	62	T5	PB1	I/O	TT_u	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN1, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT	ADC12_INP5, COMP1_INM
36	G5	48	L6	M6	58	63	R6	PB2	I/O	FT_ha	-	RTC_OUT, SAI1_D1, DFSDM1_CKIN1, SAI1_SD_A, SPI3_MOSI/I2S3_SDO, SAI4_SD_A, QUADSPI_CLK, SAI4_D1, EVENTOUT	COMP1_INP
-	-	-	-	-	-	64	P5	PI15	I/O	FT	-	LCD_G2, LCD_R0, EVENTOUT	-
-	-	-	J4	-	-	65	N6	PJ0	I/O	FT	-	LCD_R7, LCD_R1, EVENTOUT	-
-	-	-	H5	-	-	66	P6	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-
-	-	-	-	-	-	67	T6	PJ2	I/O	FT	-	LCD_R3, EVENTOUT	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	-	-	-	68	U6	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	-	-	69	U7	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	-	49	M6	R6	59	70	T7	PF11	I/O	FT_a	-	SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, DCMI_D12, EVENTOUT	ADC1_INP2
-	-	50	N6	P6	60	71	R7	PF12	I/O	FT_ha	-	FMC_A6, EVENTOUT	ADC1_INN2, ADC1_INP6
-	-	51	M11	M8	61	72	J3	VSS	S	-	-	-	-
-	-	52	-	N8	62	73	H5	VDD	S	-	-	-	-
-	-	53	G7	N6	63	74	P7	PF13	I/O	FT_ha	-	DFSDM1_DATIN6, I2C4_SMBA, FMC_A7, EVENTOUT	ADC2_INP2
-	-	54	H7	R7	64	75	P8	PF14	I/O	FT_fha	-	DFSDM1_CKIN6, I2C4_SCL, FMC_A8, EVENTOUT	ADC2_INN2, ADC2_INP6
-	-	55	J7	P7	65	76	R9	PF15	I/O	FT_fh	-	I2C4_SDA, FMC_A9, EVENTOUT	-
-	-	56	K7	N7	66	77	T8	PG0	I/O	FT_h	-	FMC_A10, EVENTOUT	-
-	-	-	M2	F6	-	-	J16	VSS	S	-	-	-	-
-	-	-	A10	-	-	-	H13	VDD	S	-	-	-	-
-	-	57	L7	M7	67	78	U8	PG1	I/O	TT_h	-	FMC_A11, EVENTOUT	OPAMP2_VINM
37	H5	58	G8	R8	68	79	U9	PE7	I/O	TT_ha	-	TIM1_ETR, DFSDM1_DATIN2, UART7_RX, QUADSPI_BK2_IO0, FMC_D4/FMC_DA4, EVENTOUT	OPAMP2_VOUT, COMP2_INM
38	J5	59	H8	P8	69	80	T9	PE8	I/O	TT_ha	-	TIM1_CH1N, DFSDM1_CKIN2, UART7_TX, QUADSPI_BK2_IO1, FMC_D5/FMC_DA5, COMP2_OUT, EVENTOUT	OPAMP2_VINM
39	K5	60	J8	P9	70	81	P9	PE9	I/O	TT_ha	-	TIM1_CH1, DFSDM1_CKOUT, UART7_RTS/UART7_DE, QUADSPI_BK2_IO2, FMC_D6/FMC_DA6, EVENTOUT	OPAMP2_VINP, COMP2_INP

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	61	C12	M9	71	82	J17	VSS	S	-	-	-	-
-	-	62	C13	N9	72	83	J13	VDD	S	-	-	-	-
40	G6	63	M8	R9	73	84	N9	PE10	I/O	FT_ha	-	TIM1_CH2N, DFSDM1_DATIN4, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7/FMC_DA7, EVENTOUT	COMP2_INM
41	H6	64	N8	P10	74	85	P10	PE11	I/O	FT_ha	-	TIM1_CH2, DFSDM1_CKIN4, SPI4_NSS, SAI2_SD_B, FMC_D8/FMC_DA8, LCD_G3, EVENTOUT	COMP2_INP
42	J6	65	L8	R10	75	86	R10	PE12	I/O	FT_h	-	TIM1_CH3N, DFSDM1_DATIN5, SPI4_SCK, SAI2_SCK_B, FMC_D9/FMC_DA9, COMP1_OUT, LCD_B4, EVENTOUT	-
43	K6	66	K8	N11	76	87	T10	PE13	I/O	FT_h	-	TIM1_CH3, DFSDM1_CKIN5, SPI4_MISO, SAI2_FS_B, FMC_D10/FMC_DA10, COMP2_OUT, LCD_DE, EVENTOUT	-
-	-	-	L12	F7	-	-	T12	VSS	S	-	-	-	-
-	-	-	H13	-	-	-	K13	VDD	S	-	-	-	-
44	G7	67	J9	P11	77	88	U10	PE14	I/O	FT_h	-	TIM1_CH4, SPI4_MOSI, SAI2_MCLK_B, FMC_D11/FMC_DA11, LCD_CLK, EVENTOUT	-
45	H7	68	N9	R11	78	89	R11	PE15	I/O	FT_h	-	TIM1_BKIN, FMC_D12/FMC_DA12, TIM1_BKIN_COMP12/ COMP_TIM1_BKIN, LCD_R7, EVENTOUT	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
46	J7	69	L9	R12	79	90	P11	PB10	I/O	FT_f	-	TIM2_CH3, HRTIM_SCOUT, LPTIM2_IN1, I2C2_SCL, SPI2_SCK/I2S2_CK, DFSDM1_DATIN7, USART3_TX, QUADSPI_BK1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-
47	K7	70	M9	R13	80	91	P12	PB11	I/O	FT_f	-	TIM2_CH4, HRTIM_SCIN, LPTIM2_ETR, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, LCD_G5, EVENTOUT	-
48	F8	71	N10	M10	81	92	U11	VCAP	S	-	-	-	-
49	E4	-	-	K7	-	93	-	VSS	S	-	-	-	-
-	-	-	M10	-	-	-	U12	VDDLDO (8)	S	-	-	-	-
50	-	72	M1	N10	82	94	L13	VDD	S	-	-	-	-
-	-	-	-	-	-	95	R12	PJ5	I/O	FT	-	LCD_R6, EVENTOUT	-
-	-	-	-	M11	83	96	T11	PH6	I/O	FT	-	TIM12_CH1, I2C2_SMBA, SPI5_SCK, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT	-
-	-	-	-	N12	84	97	U13	PH7	I/O	FT_fa	-	I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT	-
-	-	-	-	M12	85	98	T13	PH8	I/O	FT_fha	-	TIM5_ETR, I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT	-
-	-	-	-	F8	-	-	-	VSS	S	-	-	-	-
-	-	-	L13	-	-	-	M13	VDD	S	-	-	-	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	-	M13	86	99	R13	PH9	I/O	FT_h	-	TIM12_CH2, I2C3_SMBA, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT	-
-	-	-	K9	L13	87	100	P13	PH10	I/O	FT_h	-	TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT	-
-	-	-	L10	L12	88	101	P14	PH11	I/O	FT_fh	-	TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT	-
-	-	-	K10	K12	89	102	R14	PH12	I/O	FT_fh	-	TIM5_CH3, I2C4_SDA, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	-	-	H12	90	-	N16	VSS	S	-	-	-	-
-	-	-	N11	J12	91	103	P17	VDD	S	-	-	-	-
51	K8	73	N12	P12	92	104	T14	PB12	I/O	FT_u	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN1, USART3_CK, FDCAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, TIM1_BKIN_COMP12, UART5_RX, EVENTOUT	
52	J8	74	L11	P13	93	105	U14	PB13	I/O	FT_u	-	TIM1_CH1N, LPTIM2_OUT, SPI2_SCK/I2S2_CK, DFSDM1_CKIN1, USART3_CTS/USART3_NSS, FDCAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, UART5_TX, EVENTOUT	OTG_HS_VBUS

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
53	H10	75	N13	R14	94	106	U15	PB14	I/O	FT_u	-	TIM1_CH2N, TIM12_CH1, TIM8_CH2N, USART1_TX, SPI2_MISO/I2S2_SDI, DFSDM1_DATIN2, USART3_RTS/ USART3_DE, UART4_RTS/UART4_DE, SDMMC2_D0, OTG_HS_DM, EVENTOUT	-
54	G10	76	M13	R15	95	107	T15	PB15	I/O	FT_u	-	RTC_REFIN, TIM1_CH3N, TIM12_CH2, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SDO, DFSDM1_CKIN2, UART4_CTS, SDMMC2_D1, OTG_HS_DP, EVENTOUT	-
55	K9	77	M12	P15	96	108	U16	PD8	I/O	FT_h	-	DFSDM1_CKIN3, SAI3_SCK_B, USART3_TX, SPDIFRX1_IN2, FMC_D13/FMC_DA13, EVENTOUT	-
56	J9	78	K11	P14	97	109	T17	PD9	I/O	FT_h	-	DFSDM1_DATIN3, SAI3_SD_B, USART3_RX, FDCAN2_RXFD_MODE, FMC_D14/FMC_DA14, EVENTOUT	-
57	H9	79	K12	N15	98	110	T16	PD10	I/O	FT_h	-	DFSDM1_CKOUT, SAI3_FS_B, USART3_CK, FDCAN2_TXFD_MODE, FMC_D15/FMC_DA15, LCD_B3, EVENTOUT	-
-	-	-	N7	-	-	-	N12	VDD	S	-	-	-	-
-	-	-	-	F9	-	-	U17	VSS	S	-	-	-	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
58	G9	80	J10	N14	99	111	R15	PD11	I/O	FT_h	-	LPTIM2_IN2, I2C4_SMBA, USART3_CTS/USART3_NSS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16, EVENTOUT	-
59	K10	81	K13	N13	100	112	R16	PD12	I/O	FT_fh	-	LPTIM1_IN1, TIM4_CH1, LPTIM2_IN1, I2C4_SCL, USART3_RTS/USART3_DE, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17, EVENTOUT	-
60	J10	82	J11	M15	101	113	R17	PD13	I/O	FT_fh	-	LPTIM1_OUT, TIM4_CH2, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-
-	-	83	-	K8	102	114	-	VSS	S	-	-	-	-
-	-	84	-	J13	103	115	N11	VDD	S	-	-	-	-
61	H8	85	J13	M14	104	116	P16	PD14	I/O	FT_h	-	TIM4_CH3, SAI3_MCLK_B, UART8_CTS, FMC_D0/FMC_DA0, EVENTOUT	-
62	G8	86	J12	L14	105	117	P15	PD15	I/O	FT_h	-	TIM4_CH4, SAI3_MCLK_A, UART8_RTS/UART8_DE, FMC_D1/FMC_DA1, EVENTOUT	-
-	-	-	-	-	-	118	N15	PJ6	I/O	FT	-	TIM8_CH2, LCD_R7, EVENTOUT	-
-	-	-	-	-	-	119	N14	PJ7	I/O	FT	-	TRGIN, TIM8_CH2N, LCD_G0, EVENTOUT	-
-	-	-	-	-	-	-	N10	VDD	S		-		-
-	-	-	-	F10	-	-	R8	VSS	S		-		-
-	-	-	-	-	-	120	N13	PJ8	I/O	FT	-	TIM1_CH3N, TIM8_CH1, UART8_TX, LCD_G1, EVENTOUT	-
-	-	-	-	-	-	121	M14	PJ9	I/O	FT	-	TIM1_CH3, TIM8_CH1N, UART8_RX, LCD_G2, EVENTOUT	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	-	-	-	122	L14	PJ10	I/O	FT	-	TIM1_CH2N, TIM8_CH2, SPI5_MOSI, LCD_G3, EVENTOUT	-
-	-	-	-	-	-	123	K14	PJ11	I/O	FT	-	TIM1_CH2, TIM8_CH2N, SPI5_MISO, LCD_G4, EVENTOUT	-
-	-	-	-	-	-	124	N8	VDD	S		-		-
-	-	-	-	G6	-	125	U1	VSS	S	-	-	-	-
-	-	-	-	-	-	-	N17 (2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	M16 (2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	M17 (2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	K15	VSS	S	-	-	-	-
-	-	-	-	-	-	-	L16(2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	L17(2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	K16 (2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	K17 (2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	L15	VSS	S	-	-	-	-
-	-	-	-	-	-	126	J14	PK0	I/O	FT	-	TIM1_CH1N, TIM8_CH3, SPI5_SCK, LCD_G5, EVENTOUT	-
-	-	-	-	-	-	127	J15	PK1	I/O	FT	-	TIM1_CH1, TIM8_CH3N, SPI5_NSS, LCD_G6, EVENTOUT	-
-	-	-	-	-	-	128	H17	PK2	I/O	FT	-	TIM1_BKIN, TIM8_BKIN, TIM8_BKIN_COMP12, TIM1_BKIN_COMP12, LCD_G7, EVENTOUT	-
-	-	87	H9	L15	106	129	H16	PG2	I/O	FT_h	-	TIM8_BKIN, TIM8_BKIN_COMP12, FMC_A12, EVENTOUT	-
-	-	88	H10	K15	107	130	H15	PG3	I/O	FT_h	-	TIM8_BKIN2, TIM8_BKIN2_COMP12, FMC_A13, EVENTOUT	-
-	-	-	-	G7	-	-	-	VSS	S	-	-	-	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	-	-	-	-	N7	VDD	S	-	-	-	-
-	-	89	F8	K14	108	131	H14	PG4	I/O	FT_h	-	TIM1_BKIN2, TIM1_BKIN2_COMP12, FMC_A14/FMC_BA0, EVENTOUT	-
-	-	90	H11	K13	109	132	G14	PG5	I/O	FT_h	-	TIM1_ETR, FMC_A15/FMC_BA1, EVENTOUT	-
-	-	91	G9	J15	110	133	G15	PG6	I/O	FT_h	-	TIM17_BKIN, HRTIM_CHE1, QUADSPI_BK1_NCS, FMC_NE3, DCMI_D12, LCD_R7, EVENTOUT	-
-	-	92	G10	J14	111	134	F16	PG7	I/O	FT_h	-	HRTIM_CHE2, SAI1_MCLK_A, USART6_CK, FMC_INT, DCMI_D13, LCD_CLK, EVENTOUT	-
-	-	93	G11	H14	112	135	F15	PG8	I/O	FT_h	-	TIM8_ETR, SPI6_NSS, USART6_RTS/USART6_DE, SPDIFRX1_IN3, ETH_PPS_OUT, FMC_SDCLK, LCD_G7, EVENTOUT	-
-	-	94	-	G12	113	136	G16	VSS	S	-	-	-	-
-	-	-	G12	-	-	-	G17	VDD50 USB	S	-	-	-	-
-	F6	95	G13	H13	114	137	F17	VDD33 USB	S	-	-	-	-
-	-	-	-	-	-	-	M5	VDD	S	-	-	-	-
63	F10	96	F9	H15	115	138	F14	PC6	I/O	FT_h	-	HRTIM_CHA1, TIM3_CH1, TIM8_CH1, DFSDM1_CKIN3, I2S2_MCK, USART6_TX, SDMMC1_D0DIR, FMC_NWAIT, SDMMC2_D6, SDMMC1_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	SWPMI_IO

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
64	E10	97	F10	G15	116	139	F13	PC7	I/O	FT_h	-	TRGIO, HRTIM_CHA2, TIM3_CH2, TIM8_CH2, DFSDM1_DATIN3, I2S3_MCK, USART6_RX, SDMMC1_D123DIR, FMC_NE1, SDMMC2_D7, SWPMI_TX, SDMMC1_D7, DCMI_D1, LCD_G6, EVENTOUT	-
65	F9	98	F12	G14	117	140	E13	PC8	I/O	FT_h	-	TRACED1, HRTIM_CHB1, TIM3_CH3, TIM8_CH3, USART6_CK, UART5_RTS/UART5_DE, FMC_NE2/FMC_NCE, SWPMI_RX, SDMMC1_D0, DCMI_D2, EVENTOUT	-
66	E9	99	F11	F14	118	141	E14	PC9	I/O	FT_fh	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, LCD_G3, SWPMI_SUSPEND, SDMMC1_D1, DCMI_D3, LCD_B2, EVENTOUT	-
-	-	-	-	G8	-	-	-	VSS	S	-	-		-
-	-	-	-	-	-	-	L5	VDD	S	-	-		-
67	D9	100	E12	F15	119	142	E15	PA8	I/O	FT_fha	-	MCO1, TIM1_CH1, HRTIM_CHB2, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, UART7_RX, TIM8_BKIN2_COMP12, LCD_B3, LCD_R6, EVENTOUT	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
68	C9	101	E11	E15	120	143	D15	PA9	I/O	FT_u	-	TIM1_CH2, HRTIM_CHC1, LPUART1_TX, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, FDCAN1_RXFD_MODE, DCMI_D0, LCD_R5, EVENTOUT	OTG_FS_VBUS
69	D10	102	E10	D15	121	144	D14	PA10	I/O	FT_u	-	TIM1_CH3, HRTIM_CHC2, LPUART1_RX, USART1_RX, FDCAN1_TXFD_MODE, OTG_FS_ID, MDIOS_MDIO, LCD_B4, DCMI_D1, LCD_B1, EVENTOUT	-
70	C10	103	F13	C15	122	145	E17	PA11	I/O	FT_u	-	TIM1_CH4, HRTIM_CHD1, LPUART1_CTS, SPI2_NSS/I2S2_WS, UART4_RX, USART1_CTS/USART1_NSS, FDCAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT	-
71	B10	104	E13	B15	123	146	E16	PA12	I/O	FT_u	-	TIM1_ETR, HRTIM_CHD2, LPUART1_RTS/LPUART1_DE, SPI2_SCK/I2S2_CK, UART4_TX, USART1_RTS/USART1_DE, SAI2_FS_B, FDCAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT	-
72	A10	105	D11	A15	124	147	C15	PA13 (JTMS/SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
73	E7	106	D13	F13	125	148	D17	VCAP	S	-	-	-	-
74	E5	107	-	F12	126	149	-	VSS	S	-	-	-	-
-	-	-	D12	-	-	-	C17	VDDLDO (8)		-	-	-	-
75	-	108	-	G13	127	150	K5	VDD	S	-	-	-	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	-	E12	128	151	D16	PH13	I/O	FT_h	-	TIM8_CH1N, UART4_TX, FDCAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-
-	-	-	-	E13	129	152	B17	PH14	I/O	FT_h	-	TIM8_CH2N, UART4_RX, FDCAN1_RX, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT	-
-	-	-	-	D13	130	153	B16	PH15	I/O	FT_h	-	TIM8_CH3N, FDCAN1_TXFD_MODE, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT	-
-	-	-	A13	E14	131	154	A16	PI0	I/O	FT_h	-	TIM5_CH4, SPI2_NSS/I2S2_WS, FDCAN1_RXFD_MODE, FMC_D24, DCMI_D13, LCD_G5, EVENTOUT	-
-	-	-	-	G9	-	-	-	VSS	S	-	-	-	-
-	-	-	B13	D14	132	155	A15	PI1	I/O	FT_h	-	TIM8_BKIN2, SPI2_SCK/I2S2_CK, TIM8_BKIN2_COMP12, FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-
-	-	-	A6	C14	133	156	B15	PI2	I/O	FT_h	-	TIM8_CH4, SPI2_MISO/I2S2_SDI, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT	-
-	-	-	B7	C13	134	157	C14	PI3	I/O	FT_h	-	TIM8_ETR, SPI2_MOSI/I2S2_SDO, FMC_D27, DCMI_D10, EVENTOUT	-
-	-	-	-	D9	135	-	-	VSS	S	-	-	-	-
-	-	-	-	C9	136	158	-	VDD	S	-	-	-	-
76	A9	109	B12	A14	137	159	B14	PA14 (JTCK/SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
77	A8	110	C11	A13	138	160	A14	PA15 (JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, HRTIM_FLT1, CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS, UART4_RTS/UART4_DE, UART7_TX, EVENTOUT	-
78	B9	111	A12	B14	139	161	A13	PC10	I/O	FT_ha	-	HRTIM_EEV1, DFSDM1_CKIN5, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, DCMI_D8, LCD_R2, EVENTOUT	-
79	B8	112	B11	B13	140	162	B13	PC11	I/O	FT_h	-	HRTIM_FLT2, DFSDM1_DATIN5, SPI3_MISO/I2S3_SDI, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC1_D3, DCMI_D4, EVENTOUT	-
80	C8	113	A11	A12	141	163	C12	PC12	I/O	FT_h	-	TRACED3, HRTIM_EEV2, SPI3_MOSI/I2S3_SDO, USART3_CK, UART5_TX, SDMMC1_CK, DCMI_D9, EVENTOUT	-
-	-	-	-	G10	-	-	-	VSS	S	-	-	-	-
81	D8	114	D10	B12	142	164	D13	PD0	I/O	FT_h	-	DFSDM1_CKIN6, SAI3_SCK_A, UART4_RX, FDCAN1_RX, FMC_D2/FMC_DA2, EVENTOUT	-
82	E8	115	C10	C12	143	165	E12	PD1	I/O	FT_h	-	DFSDM1_DATIN6, SAI3_SD_A, UART4_TX, FDCAN1_TX, FMC_D3/FMC_DA3, EVENTOUT	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
83	B7	116	E9	D12	144	166	D12	PD2	I/O	FT_h	-	TRACED2, TIM3_ETR, UART5_RX, SDMMC1_CMD, DCMI_D11, EVENTOUT	-
84	C7	117	D9	D11	145	167	B12	PD3	I/O	FT_h	-	DFSDM1_CKOUT, SPI2_SCK/I2S2_CK, USART2_CTS/USART2_NSS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT	-
85	D7	118	C9	D10	146	168	A12	PD4	I/O	FT_h	-	HRTIM_FLT3, SAI3_FS_A, USART2_RTS/USART2_DE, FDCAN1_RXFD_MODE, FMC_NOE, EVENTOUT	-
86	B6	119	A9	C11	147	169	A11	PD5	I/O	FT_h	-	HRTIM_EEV3, USART2_TX, FDCAN1_TXFD_MODE, FMC_NWE, EVENTOUT	-
-	-	120	-	D8	148	170	-	VSS	S	-	-	-	-
-	-	121	-	C8	149	171	-	VDD	S	-	-	-	-
87	C6	122	B9	B11	150	172	B11	PD6	I/O	FT_h	-	SAI1_D1, DFSDM1_CKIN4, DFSDM1_DATIN1, SPI3_MOSI/I2S3_SDO, SAI1_SD_A, USART2_RX, SAI4_SD_A, FDCAN2_RXFD_MODE, SAI4_D1, SDMMC2_CK, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT	-
88	D6	123	D8	A11	151	173	C11	PD7	I/O	FT_h	-	DFSDM1_DATIN4, SPI1_MOSI/I2S1_SDO, DFSDM1_CKIN1, USART2_CK, SPDIFRX1_IN1, SDMMC2_CMD, FMC_NE1, EVENTOUT	-
-	-	-	-	-	-	174	D11	PJ12	I/O	FT	-	TRGOUT, LCD_G3, LCD_B0, EVENTOUT	-
-	-	-	-	-	-	175	E10	PJ13	I/O	FT	-	LCD_B4, LCD_B1, EVENTOUT	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	-	-	-	176	D10	PJ14	I/O	FT	-	LCD_B2, EVENTOUT	-
-	-	-	-	-	-	177	B10	PJ15	I/O	FT	-	LCD_B3, EVENTOUT	-
-	-	-	-	H6	-	-	-	VSS	S	-	-	-	-
-	-	-	A7	-	-	-	-	VDD	S	-	-	-	-
-	-	124	C8	C10	152	178	A10	PG9	I/O	FT_h	-	SPI1_MISO/I2S1_SDI, USART6_RX, SPDIFRX1_IN4, QUADSPI_BK2_IO2, SAI2_FS_B, FMC_NE2/FMC_NCE, DCMI_VSYNC, EVENTOUT	-
-	-	125	A8	B10	153	179	A9	PG10	I/O	FT_h	-	HRTIM_FLT5, SPI1_NSS/I2S1_WS, LCD_G3, SAI2_SD_B, FMC_NE3, DCMI_D2, LCD_B2, EVENTOUT	-
-	-	126	B8	B9	154	180	B9	PG11	I/O	FT_h	-	LPTIM1_IN2, HRTIM_EEV4, SPI1_SCK/I2S1_CK, SPDIFRX1_IN1, SDMMC2_D2, ETH_MII_TX_EN/ETH_RMII_TX_EN, DCMI_D3, LCD_B3, EVENTOUT	-
-	-	127	E8	B8	155	181	C9	PG12	I/O	FT_h	-	LPTIM1_IN1, HRTIM_EEV5, SPI6_MISO, USART6_RTS/USART6_DE, SPDIFRX1_IN2, LCD_B4, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_NE4, LCD_B1, EVENTOUT	-
-	-	128	D7	A8	156	182	D9	PG13	I/O	FT_h	-	TRACED0, LPTIM1_OUT, HRTIM_EEV10, SPI6_SCK, USART6_CTS/USART6_NSS, ETH_MII_TXD0/ETH_RMII_TXD0, FMC_A24, LCD_R0, EVENTOUT	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	129	C7	A7	157	183	D8	PG14	I/O	FT_h	-	TRACED1, LPTIM1_ETR, SPI6_MOSI, USART6_TX, QUADSPI_BK2_IO3, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_A25, LCD_B0, EVENTOUT	-
-	-	130	-	D7	158	184	-	VSS	S	-	-	-	-
-	-	131	-	C7	159	185	-	VDD	S	-	-	-	-
-	-	-	-	-	-	186	C8	PK3	I/O	FT	-	LCD_B4, EVENTOUT	-
-	-	-	-	-	-	187	B8	PK4	I/O	FT	-	LCD_B5, EVENTOUT	-
-	-	-	-	-	-	188	A8	PK5	I/O	FT	-	LCD_B6, EVENTOUT	-
-	-	-	-	-	-	189	C7	PK6	I/O	FT	-	LCD_B7, EVENTOUT	-
-	-	-	-	-	-	190	D7	PK7	I/O	FT	-	LCD_DE, EVENTOUT	-
-	-	-	-	H7	-	-	-	VSS	S	-	-	-	-
-	-	132	E7	B7	160	191	D6	PG15	I/O	FT_h	-	USART6_CTS/USART6_NSS, FMC_SDNCAS, DCMI_D13, EVENTOUT	-
89	A7	133	F7	A10	161	192	C6	PB3(JTDO/TRACESWO)	I/O	FT	-	JTDO/TRACESWO, TIM2_CH2, HRTIM_FLT4, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, SPI6_SCK, SDMMC2_D2, CRS_SYNC, UART7_RX, EVENTOUT	-
90	A6	134	B6	A9	162	193	B7	PB4(NJTRST)	I/O	FT	-	NJTRST, TIM16_BKIN, TIM3_CH1, HRTIM_EEV6, SPI1_MISO/I2S1_SDI, SPI3_MISO/I2S3_SDI, SPI2_NSS/I2S2_WS, SPI6_MISO, SDMMC2_D3, UART7_TX, EVENTOUT	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
91	C5	135	C6	A6	163	194	A5	PB5	I/O	FT	-	TIM17_BKIN, TIM3_CH2, HRTIM_EEV7, I2C1_SMBA, SPI1_MOSI/I2S1_SDO, I2C4_SMBA, SPI3_MOSI/I2S3_SDO, SPI6_MOSI, FDCAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, UART5_RX, EVENTOUT	-
-	-	-	-	H8	-	-	-	VSS	S	-	-	-	-
92	B5	136	A5	B6	164	195	B5	PB6	I/O	FT_f	-	TIM16_CH1N, TIM4_CH1, HRTIM_EEV8, I2C1_SCL, CEC, I2C4_SCL, USART1_TX, LPUART1_TX, FDCAN2_TX, QUADSPI_BK1_NCS, DFSDM1_DATIN5, FMC_SDNE1, DCMI_D5, UART5_TX, EVENTOUT	-
93	A5	137	D6	B5	165	196	C5	PB7	I/O	FT_fa	-	TIM17_CH1N, TIM4_CH2, HRTIM_EEV9, I2C1_SDA, I2C4_SDA, USART1_RX, LPUART1_RX, FDCAN2_TXFD_MODE, DFSDM1_CKIN5, FMC_NL, DCMI_VSYNC, EVENTOUT	PVD_IN
94	D5	138	E6	D6	166	197	E8	BOOT0	I	B	-	-	VPP
95	B4	139	B5	A5	167	198	D5	PB8	I/O	FT_fh	-	TIM16_CH1, TIM4_CH3, DFSDM1_CKIN7, I2C1_SCL, I2C4_SCL, SDMMC1_CKIN, UART4_RX, FDCAN1_RX, SDMMC2_D4, ETH_MII_TXD3, SDMMC1_D4, DCMI_D6, LCD_B6, EVENTOUT	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
96	A4	140	C5	B4	168	199	D4	PB9	I/O	FT_fh	-	TIM17_CH1, TIM4_CH4, DFSDM1_DATIN7, I2C1_SDA, SPI2_NSS/I2S2_WS, I2C4_SDA, SDMMC1_CDIR, UART4_TX, FDCAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT	-
97	D4	141	D5	A4	169	200	C4	PE0	I/O	FT_h	-	LPTIM1_ETR, TIM4_ETR, HRTIM_SCIN, LPTIM2_ETR, UART8_RX, FDCAN1_RXFD_MODE, SAI2_MCLK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	C4	142	D4	A3	170	201	B4	PE1	I/O	FT_h	-	LPTIM1_IN2, HRTIM_SCOUT, UART8_TX, FDCAN1_TXFD_MODE, FMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	-	-	-	-	-	A7	VCAP	S	-	-	-	-
99	-	-	-	D5	-	202	-	VSS	S	-	-	-	-
-	F7	143	C4	C6	171	203	E7	PDR_ON	I	FT	-	-	-
-	F4	-	B4	-	-	-	A6	VDDLDO (8)	S	-	-	-	-
100	-	144	-	C5	172	204	-	VDD	S	-	-	-	-
-	-	-	-	D4	173	205	A4	PI4	I/O	FT_h	-	TIM8_BKIN, SAI2_MCLK_A, TIM8_BKIN_COMP12, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	-	-	C4	174	206	A3	PI5	I/O	FT_h	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-

Table 9. Pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	A4	C3	175	207	A2	PI6	I/O	FT_h	-	TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	-	E2	C2	176	208	B3	PI7	I/O	FT_h	-	TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-
-	-	-	-	H9	-	-	-	VSS	S	-	-	-	-
-	-	-	-	K9	-	-	-	VSS	S	-	-	-	-
-	-	-	-	K10	-	-	M15	VSS	S	-	-	-	-

1. When this pin/ball was previously configured as an oscillator, the oscillator function is kept during and after a reset. This is valid for all resets except for power-on reset.
2. This ball should remain floating.
3. This ball should not remain floating. It can be connected to VSS or VDD. It is reserved for future use.
4. This ball should be connected to V_{SS}.
5. Pxy_C and Pxy pins/balls are two separate pads (analog switch open). The analog switch is configured through a SYSCFG register. Refer to the product reference manual for a detailed description of the switch configuration bits.
6. There is a direct path between Pxy_C and Pxy pins/balls, through an analog switch. Pxy alternate functions are available on Pxy_C when the analog switch is closed. The analog switch is configured through a SYSCFG register. Refer to the product reference manual for a detailed description of the switch configuration bits.
7. VREF+ pin, and consequently the internal voltage reference, are not available on the TFBGA100 package. On this package, this pin is double-bonded to VDDA which can be connected to an external reference. The internal voltage reference buffer is not available and must be kept disabled
8. When it is not available on a package, the VDDLDO pin is internally tied to VDD.